ON Semiconductor®

DAP011/DAP011C

PWM Current-Mode Controller for High-Power Universal Off-Line Supplies

Housed in an SO−14 package, the DAP011/DAP011C represents an enhanced version of the Maximus, DAP008, controller. Due to its high drive capability, *SpeedKing* drives large gate−charge MOSFETs which, together with internal ramp compensation and a user selectable frequency jittering, ease the design of modern AC/DC adapters.

With an internal structure operating at a fixed 65/100 kHz frequency, the controller directly connects to the high−voltage rail for a loss less and clean startup sequence. Current−mode control also provides an excellent input audio−susceptibility and inherent pulse−by−pulse control. Internal ramp compensation easily prevents subharmonic oscillations from taking place in continuous conduction mode designs.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at a user adjustable low peak current, no acoustic noise takes place. Due to a proprietary SoftSkip technique, the absence of sharp transitions during skip mode significantly reduces acoustical noise.

The DAP011/DAP011C features an efficient protective circuitry which, in presence of an overcurrent condition, disables the output pulses while the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto−recovers. By implementing a timer to acknowledge a fault condition, independently from the auxiliary supply, the designer's task is eased when stringent fault mode conditions need to be met.

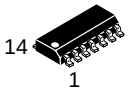
A dedicated input helps triggering a latch−off circuitry which permanently disables output pulses.

Features

- Current−Mode Control with Adjustable Skip−Cycle Capability
- Internal Ramp Compensation
- Adjustable Frequency Jittering for Better EMI Signature
- Auto−Recovery Internal Output Short−Circuit Protection
- Adjustable Timer for Improved Short−Circuit Protection
- Dedicated Latch Input
- +500 mA/−800 mA Peak Current Capability
- Fixed Frequency Versions at 65/100 kHz
- 5.0 V – 5.0 mA Reference Voltage
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- Extremely Low No−Load Standby Power
- Adjustable Soft−Start
- This is a Pb−Free Device*

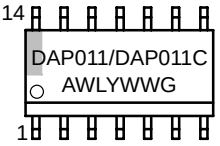
Typical Applications

- High Power AC/DC Converters for TVs, Set−Top Boxes, etc.
- Offline Adapters for Notebooks
- All Power Supplies



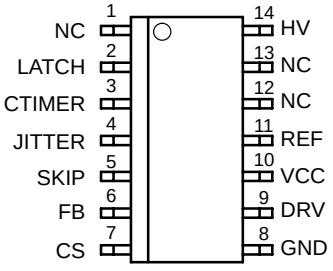
SOIC−14
D SUFFIX
CASE 751A

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



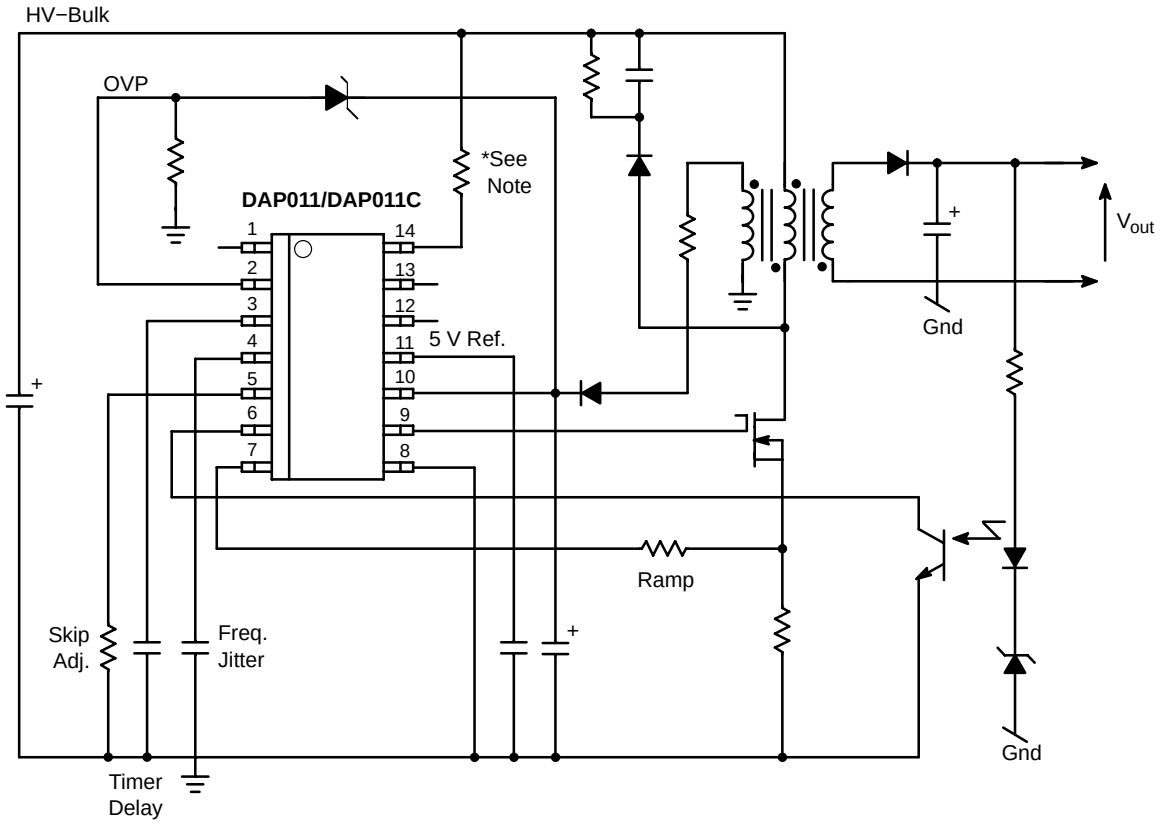
(Top View)

ORDERING INFORMATION

Device	fosc	Package	Shipping†
DAP011 DAP011C	(65 kHz) (100 kHz)	SO−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



*This resistor prevents from negatively biasing the HV pin (14) at power−off. Typical value is 4.7 kΩ.

Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	NC	−	−
2	Latch	Input voltage to latch comparator	By bringing this pin above 3.0 V, e.g. via a Zener or an NTC, the circuit permanently latches−off.
3	CTimer	Timer/soft−start delay	Wiring a capacitor to ground helps selecting the timer duration. 10% of this duration fixes the soft−start period.
4	Jitter	Frequency jittering speed	This pin offers a way to adjust the frequency modulation pace.
5	Skip	Skip cycle adjustment	By connecting a resistor to ground, it becomes possible to alter the default skip cycle level.
6	FB	Feedback pin	Hooking an optocoupler collector to this pin will allow regulation.
7	CS	Current sense + ramp compensation	This pin monitors the primary peak current but also offers a mean to introduce ramp compensation.
8	GND	−	The controller ground.
9	DRV	Driver output	The driver’s output to an external MOSFET.
10	VCC	Supplies the controller	This pin is connected to an external auxiliary voltage.
11	Ref.	Reference voltage	This pin delivers 5.0 V and sources up to 5.0 mA.
12	NC	−	Non−connected for improved creepage.
13	NC	−	Non−connected for improved creepage.
14	HV	High−voltage input	Connected to the bulk capacitor, this pin powers the internal current source to deliver a startup current.

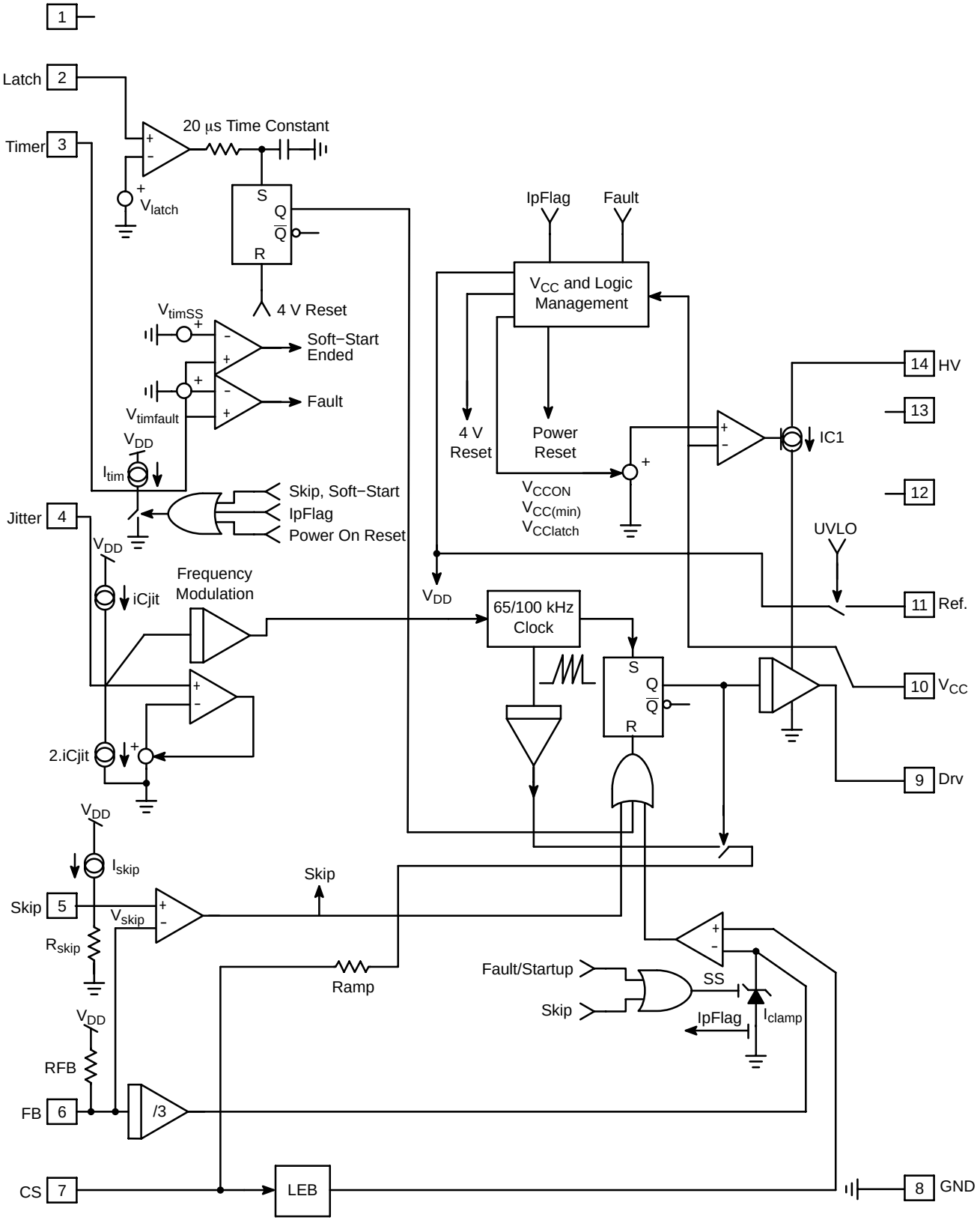


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, V_{CC} Pin, Continuous Voltage	V_{CC}	20	V
Transient Power Supply Voltage, Duration < 10 ms, IV_{CC} < 20 mA	−	25	V
Maximum Voltage on Low Power Pins (Except Pin 9, Pin 10, Pin 5 and Pin 14)	−	−0.3 to 10	V
Maximum Voltage on Pin 5	−	5.0	V
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	120	°C/W
Thermal Reference Junction−to−Lead (Note 3)	P_{si} J_L	40	°C/W
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, HBM Model (All Pins Except HV)	−	2.0	kV
ESD Capability, Machine Model	−	200	V
Maximum Voltage on Pin 14 (HV)	−	−0.3 to 500	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per Mil−Std−883, Method 3015. Machine Model Method 200 V
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. Minimum Pad FR4 Board 1 oz Copper.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −5°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted.)

Characteristic		Symbol	Pin	Min	Typ	Max	Unit
SUPPLY SECTION							
V_{CC} Increasing Level at which the Current Source Turns−Off		V_{CCON}	10	11.8	12.8	13.8	V
V_{CC} Level at which Output Pulses are Stopped		$V_{CC(min)}$	10	8.0	9.0	10	V
V_{CC} Decreasing Level at which the Latch−Off Phase Ends		$V_{CClatch}$	10	−	6.5	−	V
Internal Latch Reset Level		$V_{CCreset}$	10	−	5.0	−	V
Minimum Voltage Difference between $V_{CClatch}$ and $V_{CCReset}$		$reset_{Hyst}$	−	1.0	−	−	V
Internal IC Consumption, No Output Load on Pin 9	DAP011 DAP011C	I_{CC1}	10	− −	1.2 1.3	− −	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 9	DAP011 DAP011C	I_{CC2}	10	− −	1.9 2.5	− −	mA
Internal IC Consumption, Latch−Off Phase		I_{CC3}	10		−	0.6	mA
Reference Voltage, I_{out} = 1.0 mA, T_J = 25°C		V_{ref1}	11	4.9	5.0	5.1	V
Reference Voltage, I_{out} = 5.0 mA		V_{ref2}	11	4.8	−	5.13	V
Maximum Output Current Capability		I_{refOut}	11	5.0	−	−	mA
Decoupling Capacitor Connected to Pin 11		C_{ref}	11	100	−	−	nF
INTERNAL STARTUP CURRENT SOURCE (T_J > −5°C) – High−voltage pin biased to 60 V DC.							
High−Voltage Current Source, V_{CC} = 10 V (Note 4)		I_{C2}	14	2.0	4.0	−	mA
High−Voltage Current Source, V_{CC} = 0		I_{C1}	14	200	500	650	μA
V_{CC} Transition Level for I_{C1} to I_{C2} Toggling Point		V_{Th}	14	−	1.8	−	V
Leakage Current for the High Voltage Source, V_{pin} 14 = 250 Vdc		I_{leak}	14	−	35	−	μA
DRIVE OUTPUT (Lothar like)							
Output Voltage Rise−Time @ C_L = 1.0 nF, 10−90% of a 12 V Output Signal		T_r	9	−	40	−	ns
Output Voltage Fall−Time @ C_L = 1.0 nF, 10−90% of a 12 V Output Signal		T_f	9	−	15	−	ns
Source Resistance		R_{OH}	9	−	12	−	Ω
Sink Resistance		R_{OL}	9	−	7.0	−	Ω
CURRENT COMPARATOR							
Input Bias Current @ 1.0 V Input Level on Pin 7		I_{IB}	7	−	0.02	−	μA
Maximum Internal Current Setpoint – T_J = 25°C		I_{Limit1}	7	0.95	1.0	1.05	V
Maximum Internal Current Setpoint – T_J from −5° to 125°C		I_{Limit2}	7	0.93	1.0	1.07	V
Default Internal Voltage Setpoint for Skip Cycle Operation		V_{Lskip}	7	−	350	−	mV
Propagation Delay from Current Detection to Gate OFF State		T_{DEL}	7	−	100	150	ns
Leading Edge Blanking Duration		T_{LEB}	7	−	200	−	ns
Soft−Start Duration, C_{timer} = 0.22 μF		TSS	−	−	10	−	ms
INTERNAL OSCILLATOR							
Oscillation Frequency	DAP011 DAP011C	f_{OSC}	−	60 92	65 100	70 108	kHz
Maximum Duty−Cycle		D_{max}	−	76	80	84	%
Frequency Jittering in Percentage of f_{OSC}	DAP011 DAP011C	f_{jitter}	−	− −	±5.0 ±6.0	− −	%
Swing Frequency with a 22 nF Capacitor to Pin 4		f_{swing}	4	−	300	−	Hz
Jittering Modulator Charging Current		I_{Cjit}	4	−	20	−	μA
Jittering Capacitor Peak Voltage		V_{CjitP}	4	−	2.15	−	V
Jittering Capacitor Valley Voltage		V_{CjitV}	4	−	0.75	−	V

4. Min. value for T_J = 125°C (See Figure 10).

ELECTRICAL CHARACTERISTICS (continued) (For typical values T_J = 25°C, for min/max values T_J = −5°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted.)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
FEEDBACK SECTION						
Internal Pullup Resistor	R_{up}	6	−	20	−	kΩ
Pin 6 to Current Setpoint Division Ratio	I_{ratio}	−	−	3.0	−	−
SKIP CYCLE GENERATION						
Internal Skip Reference Current	I_{skip}	5	−	40	−	μA
Pin 5 Internal Output Impedance (Note 5)	Z_{out}	5	−	25	−	kΩ
Default Skip Mode Level	V_{skip}	5	−	1.0	−	V
INTERNAL RAMP COMPENSATION						
Internal Ramp Level @ 25°C (Note 6)	V_{ramp}	7	−	1.8	−	V
Internal Ramp Resistance to CS Pin	R_{ramp}	7	−	20	−	kΩ
PROTECTIONS						
Latching Level Input	V_{latch}	2	2.85	3.05	3.25	V
Delay before Latch Confirmation	$T_{latch-del}$	−	−	20	−	μs
Timer Level Completion	$V_{timFault}$	3	−	4.3	−	V
Timer Capacitor Charging Current	I_{tim}	3	−	10	−	μA
Timer Length, C_{timer} = 0.22 μF Typical	T_{imerL}	3	−	100	−	ms
Temperature Shutdown	T_{SD}	−	140	−	−	°C
Temperature Shutdown Hysteresis	T_{SD_hys}	−	−	40	−	°C

5. Maximum voltage on Pin 5 is 5.0 V.
6. A 15 kΩ resistor is connected from Pin 7 to the ground for the measurement.

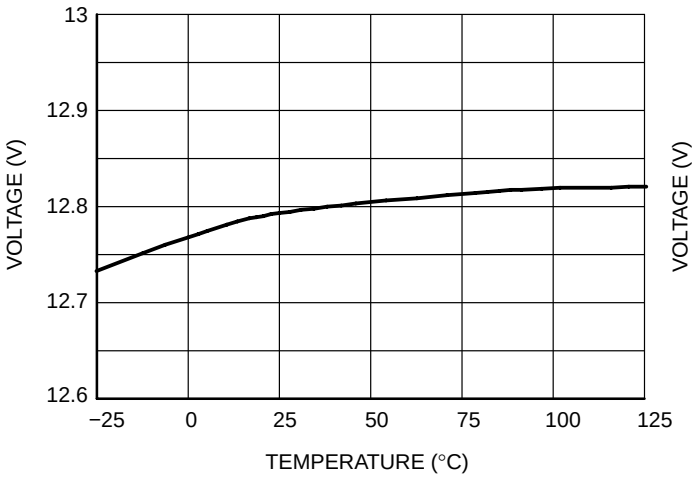


Figure 3. V_{CCon} Voltage versus Temperature

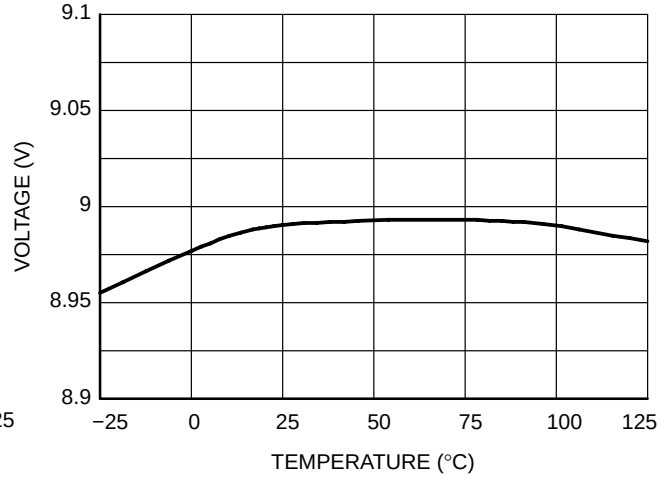


Figure 4. V_{CCmin} Voltage versus Temperature

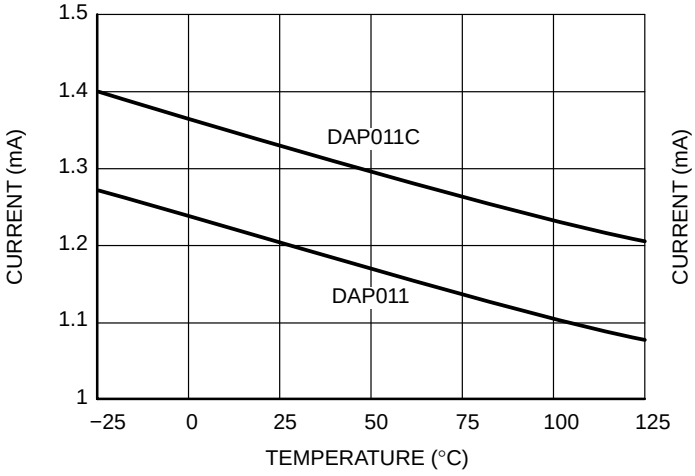


Figure 5. Current Consumption I_{CC1} versus Temperature (Driver Unloaded)

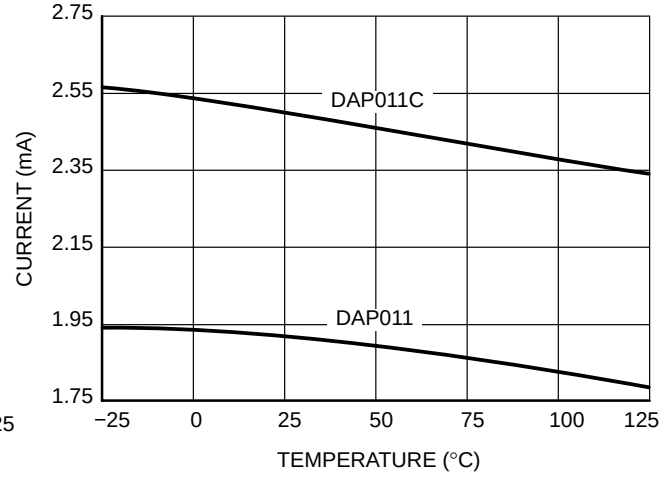


Figure 6. Current Consumption I_{CC2} versus Temperature (Driver Loaded with 1 nF)

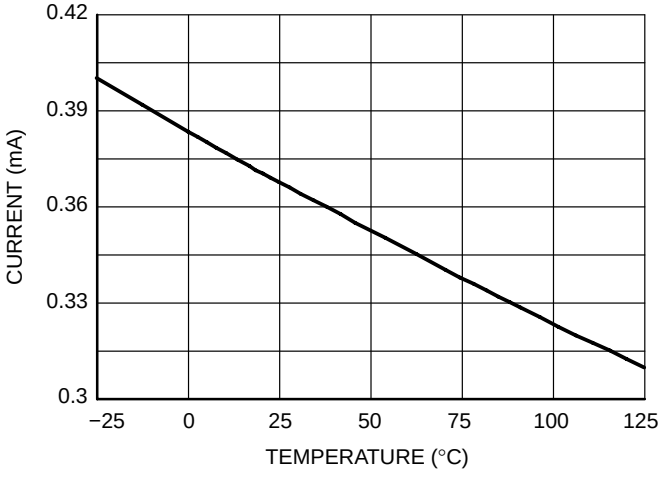


Figure 7. Current Consumption in Latch−off Phase versus Temperature

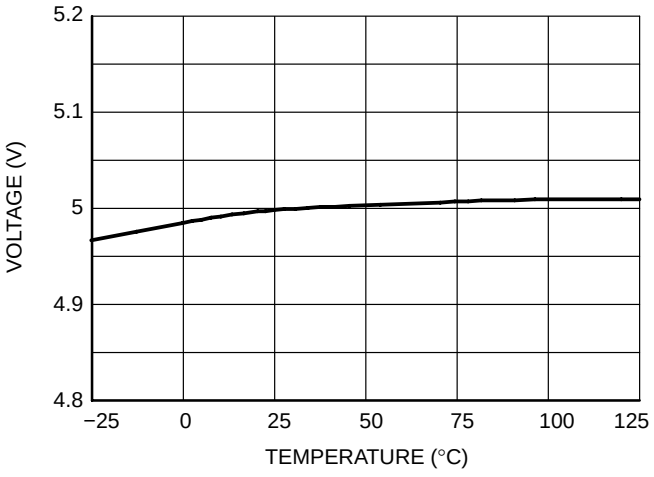


Figure 8. 5 mA Loaded Reference Voltage Evolution versus Temperature

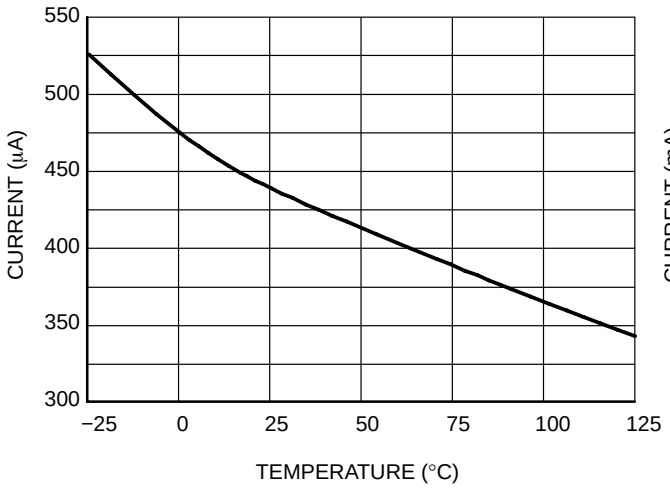


Figure 9. High Voltage Current Source Level Evolution versus Temperature when V_{CC} = 0 V

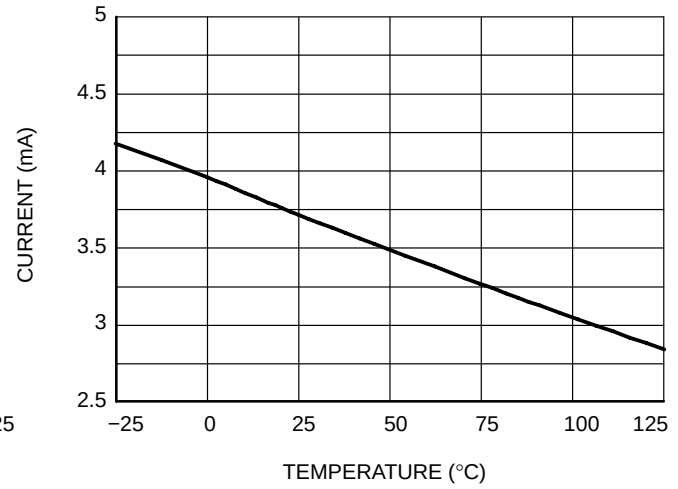


Figure 10. High Voltage Current Source Level Evolution versus Temperature when V_{CC} = 10 V

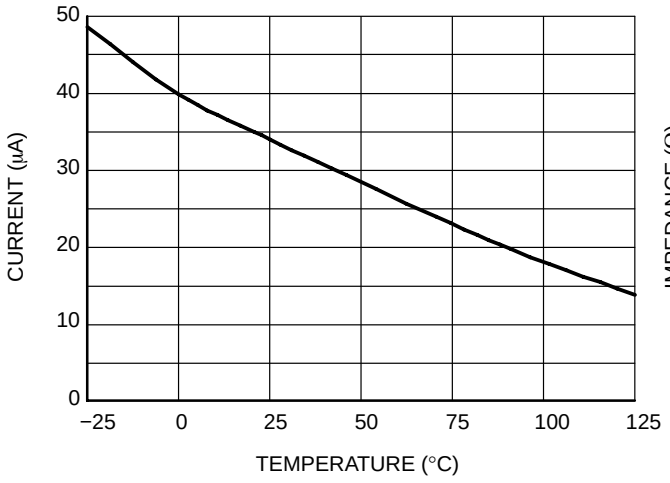


Figure 11. High Voltage Current Source Leakage versus Temperature

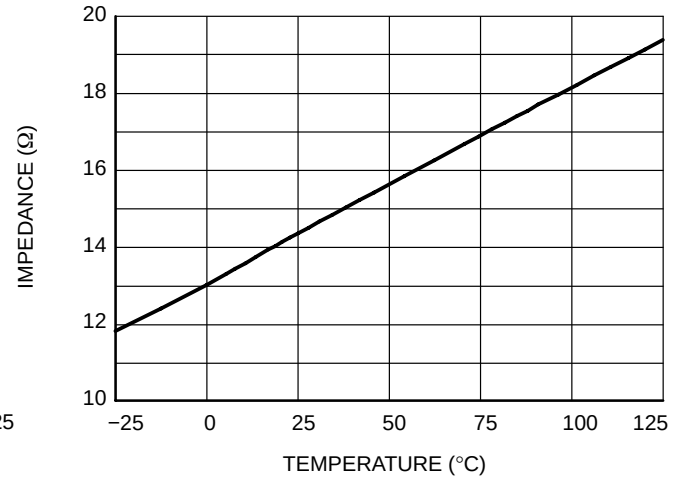


Figure 12. Driver Source Output Impedance Evolution versus Temperature

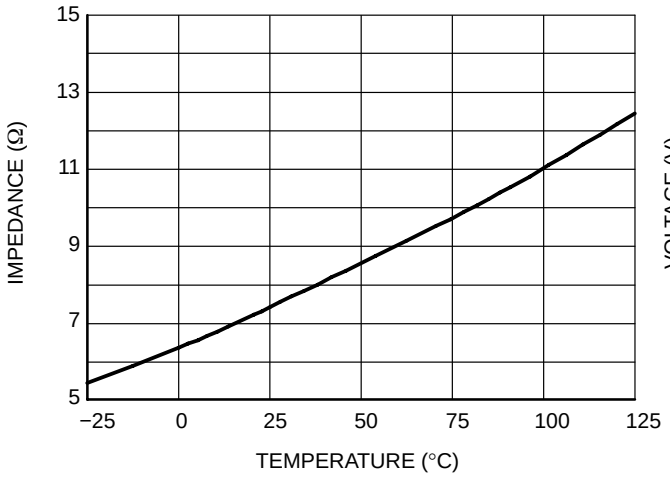


Figure 13. Driver Sink Impedance Evolution versus Temperature

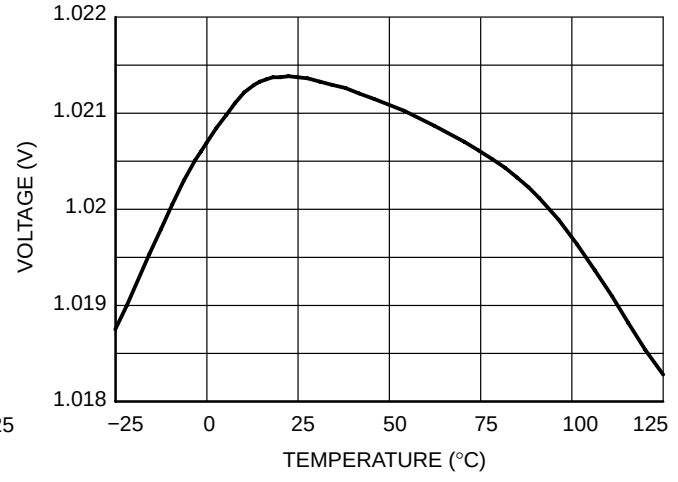


Figure 14. Maximum Peak Current Limit Evolution with Temperature

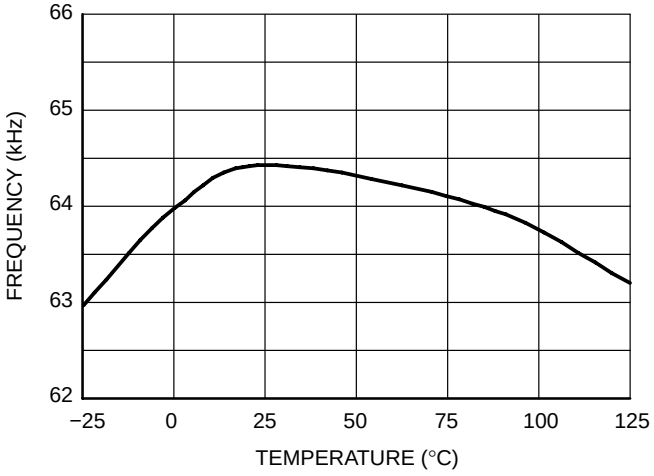


Figure 15. DAP011 Oscillator Frequency with Temperature

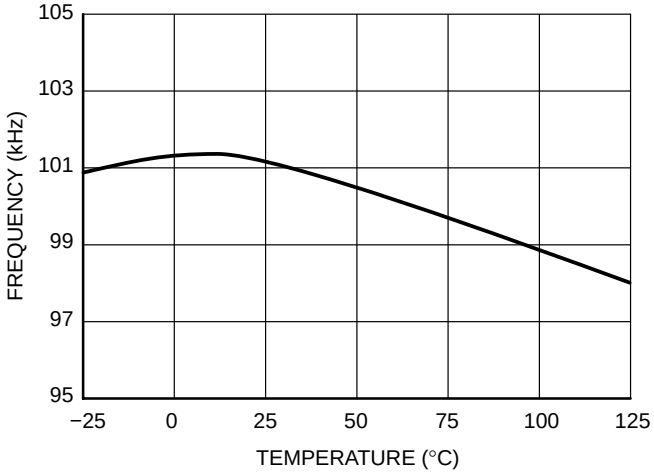


Figure 16. DAP011C Oscillator Frequency with Temperature

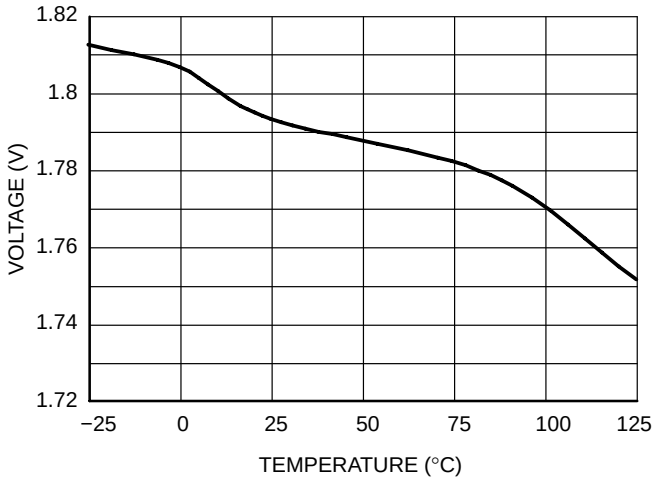


Figure 17. Ramp Compensation Voltage Evolution with Temperature

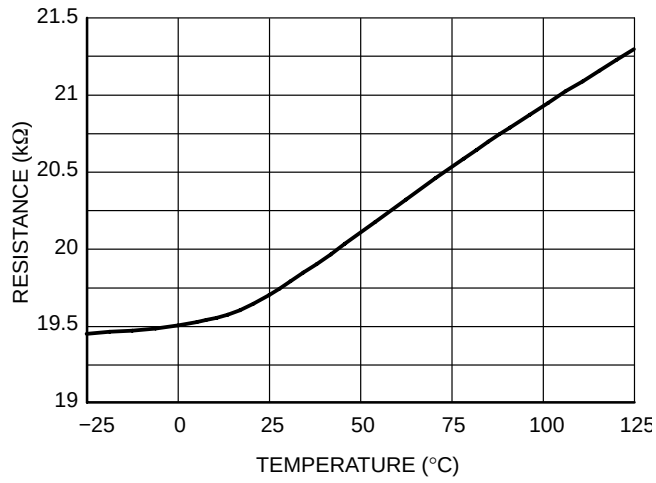


Figure 18. Ramp Compensation Resistor Value Evolution with Temperature

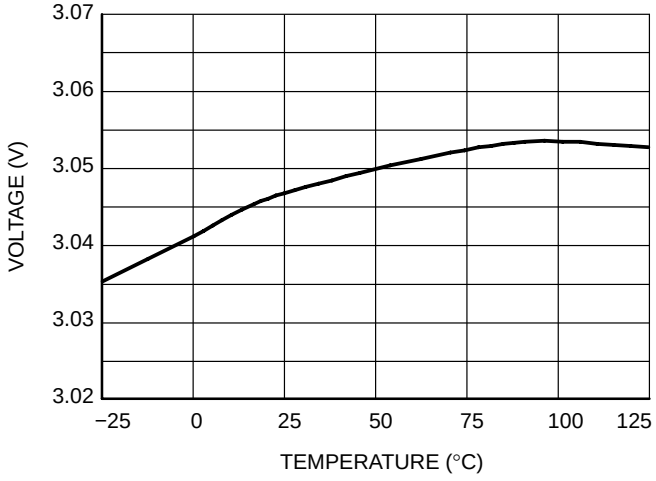


Figure 19. Latch Level Evolution with Temperature

APPLICATION INFORMATION

Introduction

SpeedKing implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC/DC adapters, open−frame power supplies etc. Due to its high voltage technology, the DAP011/DAP011C incorporates all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as an adjustable EMI jittering and a fault timer.

- Current−mode operation with internal ramp compensation: implementing peak current mode control, the DAP011/DAP011C offers an internal ramp compensation signal that can easily by summed up to the sensed current. Subharmonic oscillations can thus be fought via the inclusion of a simple resistor.
- Internal high−voltage startup switch: reaching a low no−load standby power represents a difficult exercise when the controller requires an external, lossy, resistor connected to the bulk capacitor. Thanks to an internal logic, the controller disables the high−voltage current source after startup which no longer hampers the consumption in no−load situations.
- EMI jittering: a dedicated pin offers the ability to vary the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis.
- Skip−cycle capability: a continuous flow of pulses in not compatible with no−load standby power requirements. Slicing the switching pattern in bunch of pulses drastically reduces overall losses but can, in certain cases, bring acoustic noise in the transformer. Thanks to a skip operation taking place at low peak currents only, no mechanical noise appears in the transformer. Also, activating the soft−start during skip cycle brings so−called SoftSkip benefits, greatly reducing acoustical noise in the transformer.
- Internal soft−start: a soft−start precludes the main power switch from being stressed upon startup. Its duration is equal to 10% of the fault timer, e.g. 10ms for a 100 ms timer duration.
- Latch input: by monitoring pin 2, the controller detects when it is brought above a latching level via a zener (OVP) or a NTC (OTP), or both. When the latch is detected, all pulses are permanently disabled and V_{CC} goes up and down, maintaining the latch condition. When the user cycles V_{CC} below 5.0 V, the controller gets reset and attempts to restart.
- Short−circuit protection: short−circuit and especially over−load protection are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the auxiliary winding level does not properly collapse in presence of an output short). Here, every time the internal 1.0 V maximum peak current limit is activated, an error flag, I_p Flag, is asserted and a time period starts, thanks to an adjustable timer. If the timer reaches completion while the error flag is still present, the controller stops the pulses and goes into a latch−off phase, operating in a low−frequency burst−mode. To limit the fault output power, a divide−by−two circuitry is installed on the V_{CC} pin and requires twice a startup sequence before another attempt to restart is. As soon as the fault disappears, the SMPS resumes operation. The latch−off phase can also be initiated, more classically, when V_{CC} drops below $V_{CC(min)}$ (9.0 V typical).

Startup Sequence

When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the V_{CC} capacitor. When the voltage on this V_{CC} capacitor reaches the V_{CCON} level (typically 12.8 V), the current source turns off, reducing the amount of power being dissipated. At this time, the V_{CC} capacitor only supplies the controller, and the auxiliary supply should take over before V_{CC} collapses below $V_{CC(min)}$. Figure 20 shows the internal arrangement of this structure:

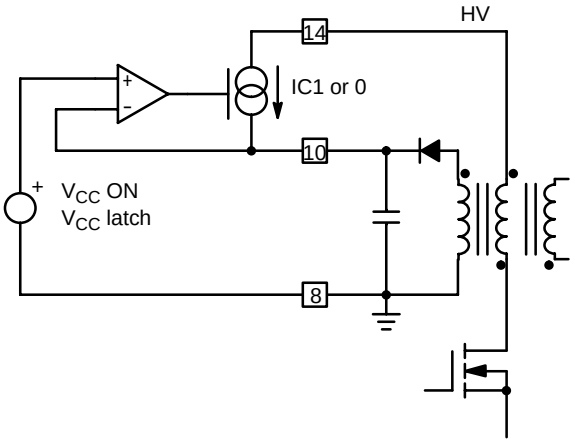


Figure 20. The Current Source brings V_{CC} above 15 V and then turns off

In some fault situations, a short−circuit can purposely occur between V_{CC} and GND. In high line conditions (VHV = 370 VDC) the current delivered by the startup device will seriously increase the junction temperature. For instance, since IC1 equals 2 mA (the minimum corresponds to the highest T_j), the device would dissipate 370 x 2 m = 740 mW. To avoid this situation, the controller includes a novel circuitry made of two startup levels, IC1 and IC2. At power−up, as long as V_{CC} is below a certain level (1.8 V typical), the source delivers IC1 (around 500 μA typical), then, when V_{CC} reaches 1.8 V, the source smoothly transitions to IC2 and delivers its nominal value. As a result, in case of short−circuit between V_{CC} and GND, the power dissipation will drop to 370 x 500 μ = 185 mW. Figure 21 portrays this particular behavior:

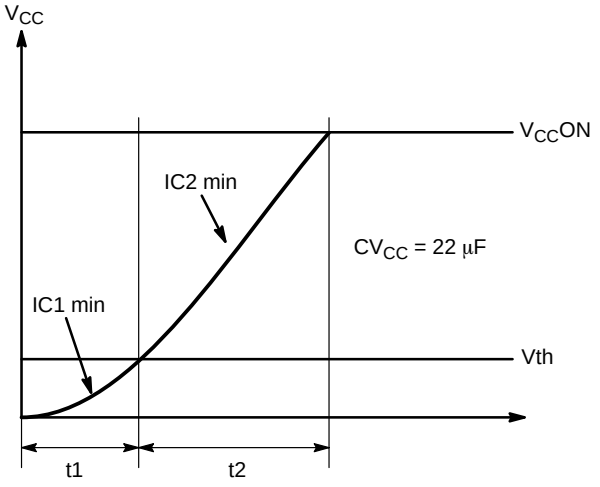


Figure 21. The Startup Source Now Features a Dual Level Startup Current

The first startup period is calculated by the formula C x V = I x t, which implies a 22 μ x 1.5 / 350 μ = 94ms startup time for the first sequence. The second sequence is obtained by changing to 2 mA with a ΔV of $V_{CCON} - V_{CCth}$ = 12.8 – 1.5 = 11.3 V, which finally leads to a second startup time of 12.8 x 22 μ / 2 m = 140 ms. The total startup time becomes 94 m + 140 m = 235 ms. Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

As soon as V_{CC} reaches V_{CCON}, drive pulses are delivered on Pin 9 and the auxiliary winding increases the voltage on the V_{CC} pin. Because the output voltage is below the target (the SMPS is starting up), the controller smoothly ramps−up the peak current to I_{max} (1.0 V / R_{sense}) which is reached after a typical soft−start period. This soft−start period lasts typically 10% of what has been selected for the fault timer via Pin 3. As soon as the peak current setpoint reaches its maximum (during the startup period but also anytime an overload occurs), an internal error flag is asserted, I_p flag, indicating that the system has reached its maximum current limit set point (I_p = I_p maximum). As soon as the error flag gets asserted, the current source on Pin 3 is activated and charges up the capacitor connected to this pin. If the error flag is still asserted when the timer capacitor has reached the threshold level V_{tim} Fault, (which is about 100 ms with a 0.22 μF typically), then the controller assumes that the power supply has really undergone a fault condition and immediately stops all pulses to enter a safe burst operation. Figure 22 depicts the V_{CC} evolution during a proper startup sequence, showing the state of the error flag:

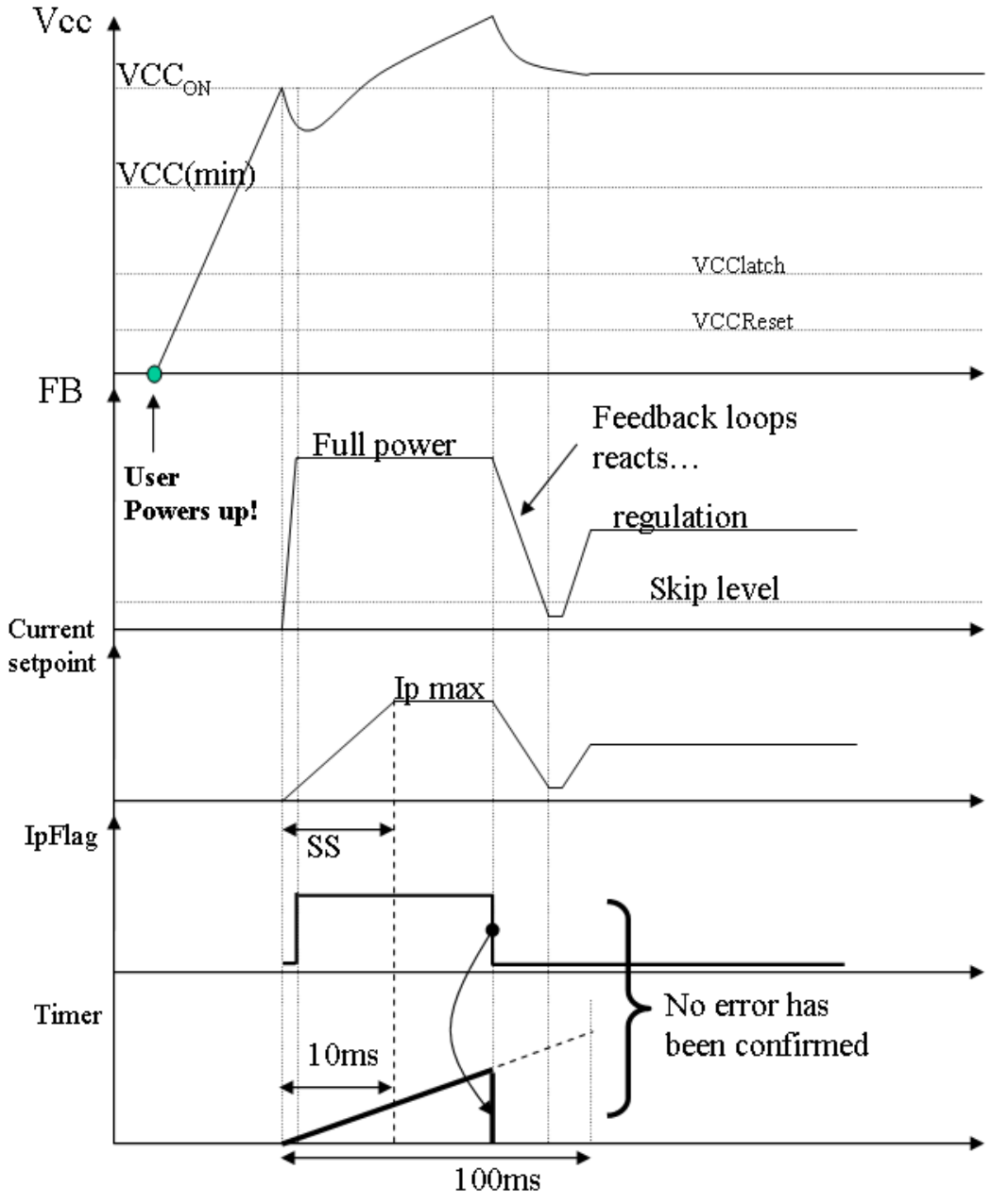


Figure 22. An Error Flag Gets Asserted as soon as the Current Setpoint Reaches its Upper limit (1.0 V/R_{sense}) Here the Timer Lasts 100 ms, a 0.22 μF Capacitor being Connected to Pin 3

Short−Circuit or Overload Mode

There can be various events that force a fault on the primary side controller. We can split them in different situation, each having a particular configuration:

1. the converter regulates but the auxiliary winding collapses: this is a typical situation linked to the usage of a constant−current / constant−voltage (CC−CV) type of controller. If the output current increases, the voltage feedback loop gives up and the current loop takes over. It means that V_{out} goes low but the feedback loop is still closed because of the output current monitoring. Therefore, seen from the primary side, there is no fault. However, there are numerous charger applications where the output voltage shall not go below a certain limit, even if the current is controlled. To cope with this situation, the controller features a precise undervoltage lockout comparator biased to a $V_{CC(min)}$ level. When this level is crossed, whatever the other pin conditions, pulses are stopped and the controller enters the safe hiccup mode, trying to restart. Figure 23 shows how the converter will behave in this situation. If the fault goes away, the SMPS resumes operation.

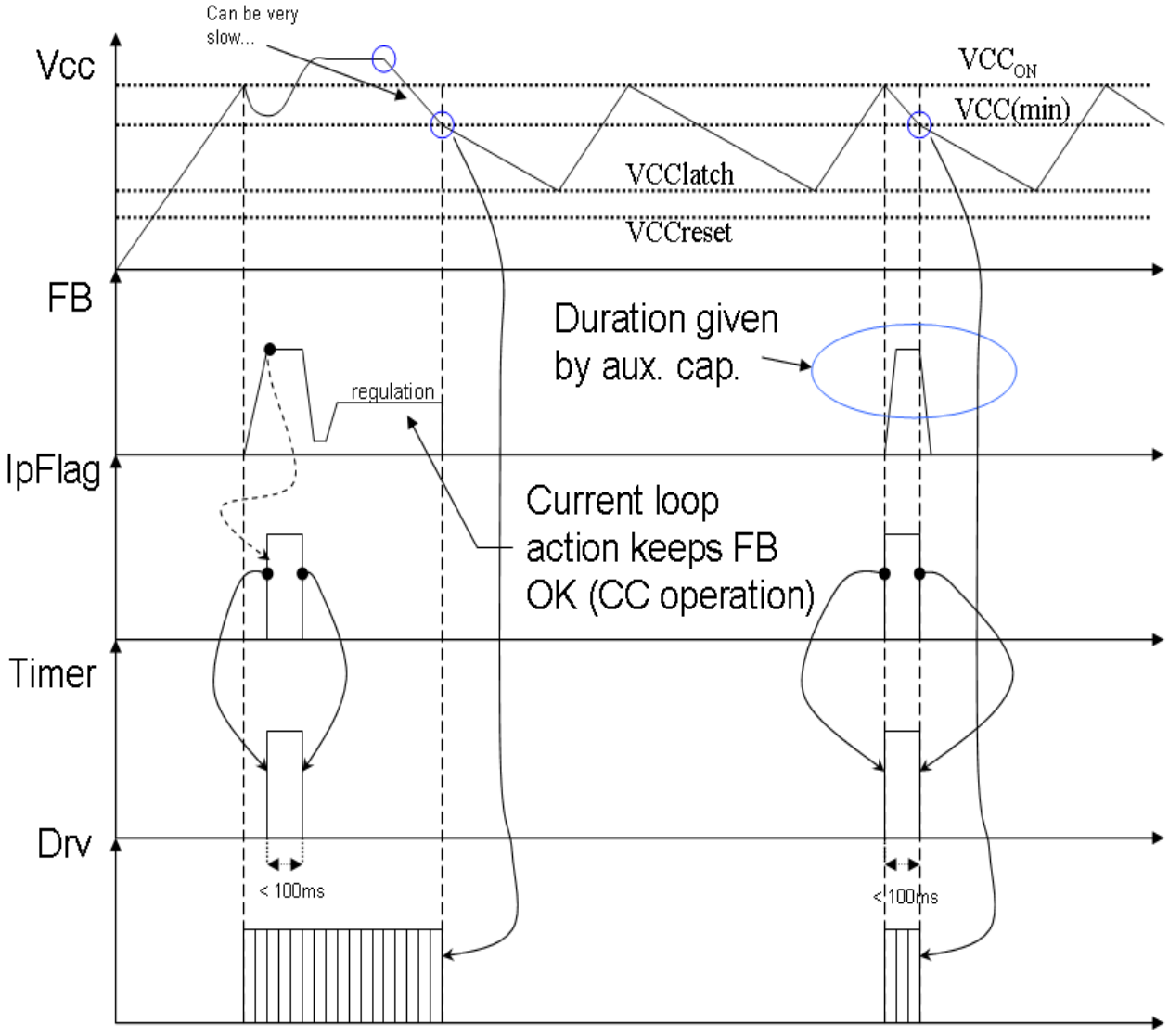


Figure 23. First Fault Mode Case, the Auxiliary Winding Collapses but Feedback is Still There

2. In the second case, the converter operates in regulation, but the output is severely overloaded. However, due to the bad coupling between the power and the auxiliary windings, the controller V_{CC} does not go low. The peak current is pushed to the maximum and the timer starts to count. Upon completion, all pulses are stopped and dual startup hiccup mode is entered. If the fault goes away, the SMPS resumes operation.

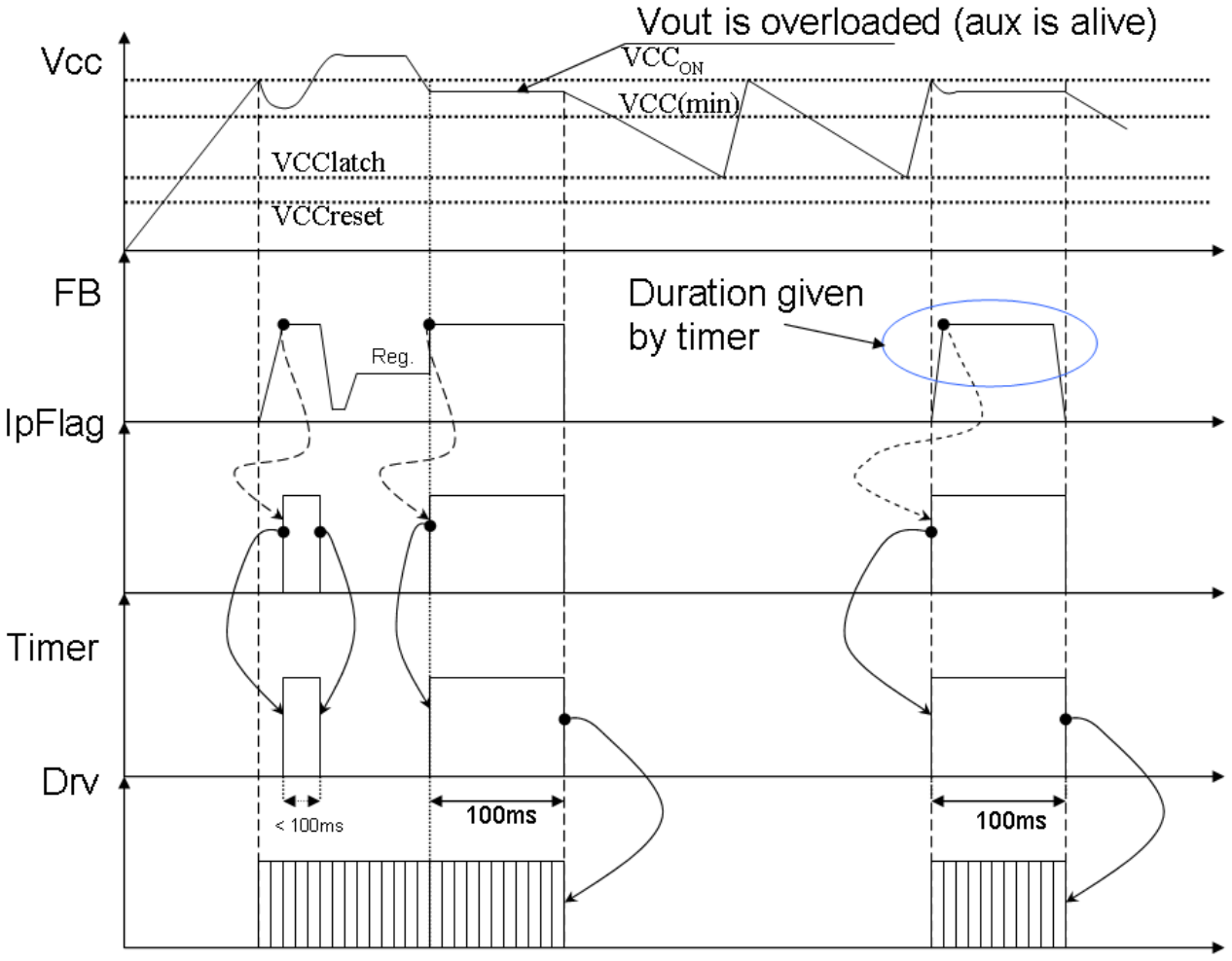


Figure 24. This Case is Similar to a Short−circuit Where V_{AUX} Does Not Collapse

3. A second case exists where the short−circuit makes the auxiliary level go below $V_{CC(min)}$. In that case, the timer length is truncated and all pulses are stopped. The double hiccup fault mode is entered and the SMPS tries to restart. When the fault is removed, the SMPS resumes operation.

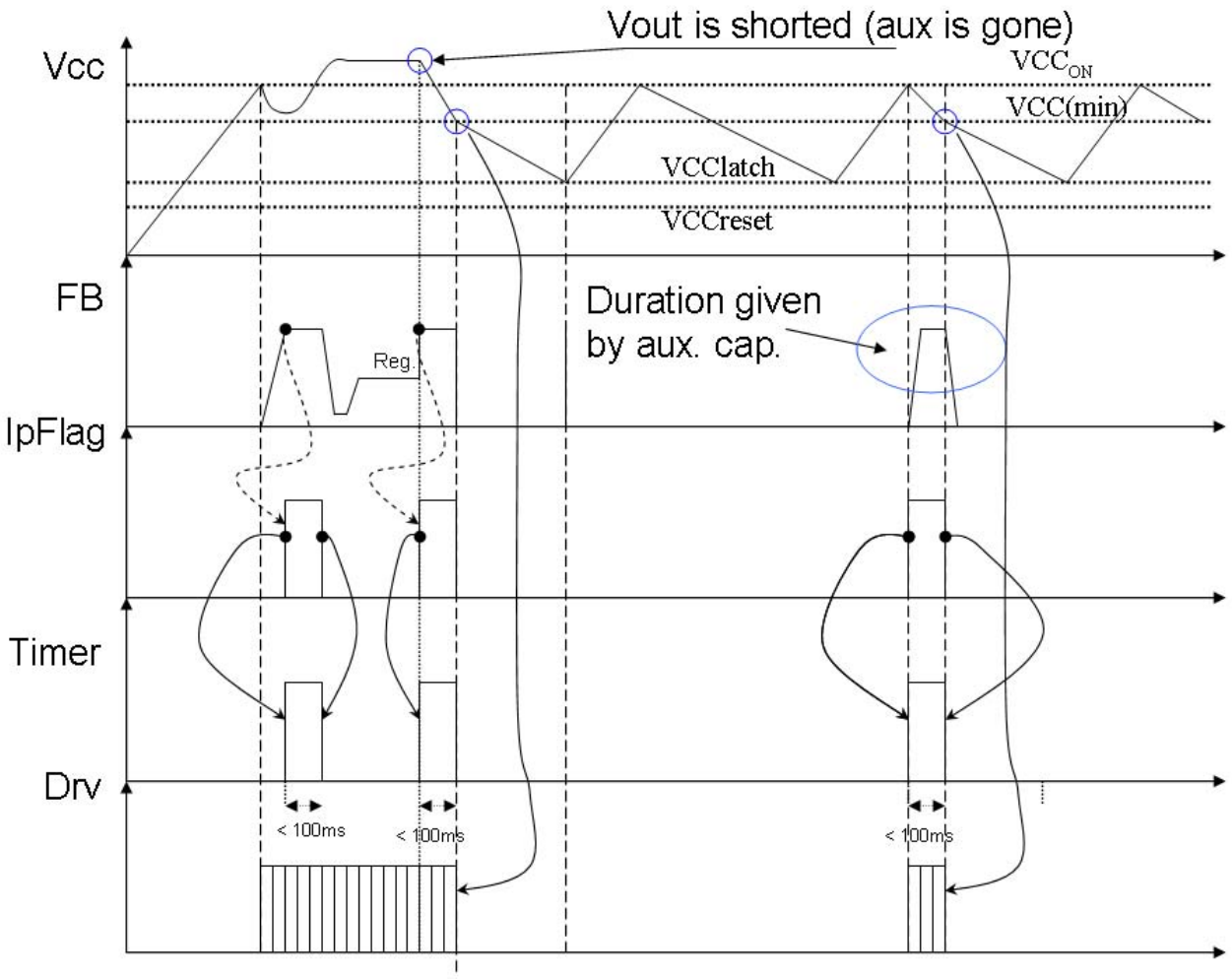


Figure 25. This Case is Similar to a Short−circuit Where V_{AUX} Does Collapse

The recurrence in hiccup mode can easily be adjusted by either reducing the timer or increasing the V_{CC} capacitor. Figure 26 details the various time portion a hiccup is made of:

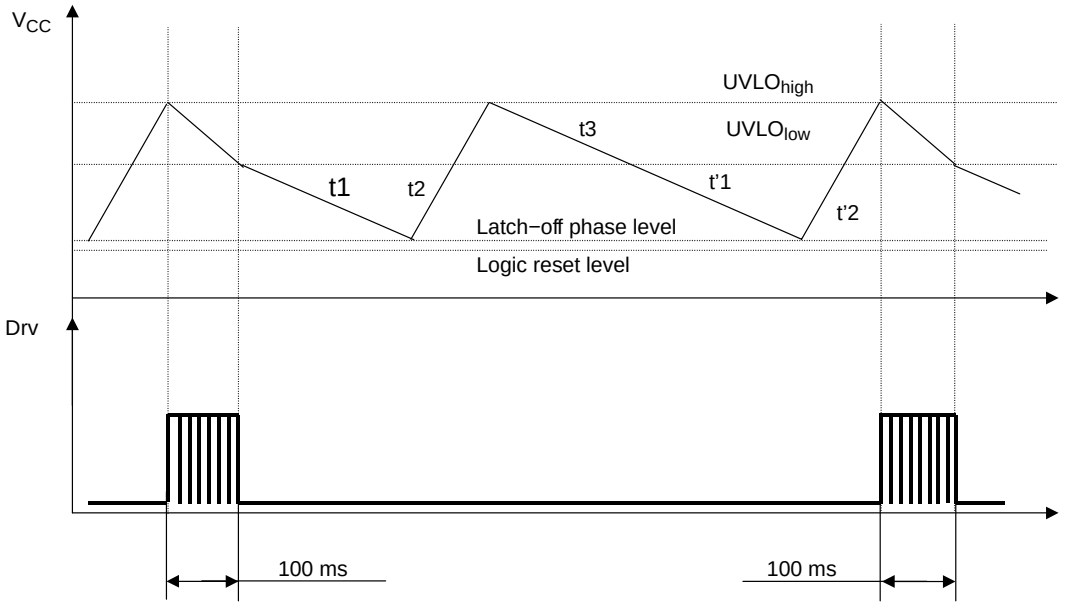


Figure 26. The Burst Period is Ensured by the V_{CC} Capacitor Charge/Discharge Cycle

If by design we have selected a 22 μF V_{CC} capacitor, it becomes easy to evaluate the burst period and its duty−cycle. This can be done by properly identifying all time events on Figure 26 and applying the classical formula:

$$t = \frac{\Delta V \cdot C}{i} \qquad \text{(eq. 1)}$$

- t1: I = I_{CC3} = 600 μA, ΔV = 9 – 6.5 = 2.5 V → t1 = 91 ms
- t2: I = 3 mA, ΔV = 12.8 – 6.5 = 6.3 → t1 = 46 ms
- t3: I = 600 μA, ΔV= 12.8 – 6.5 = 6.3 V → t1 = 231ms
- t'1 = t1 = 91 ms
- t'2 = t2 = 46 ms

The total period duration is thus the sum of all these events which leads to T_{fault} = 505 ms. If T_{pulse} = 100 ms, then our burst duty−cycle equals 100/(505+100) ≈ 16.5%, which is good. Should the user like to further decrease or, to the contrary, increase this duty−cycle, changing the V_{CC} capacitor is an easy job.

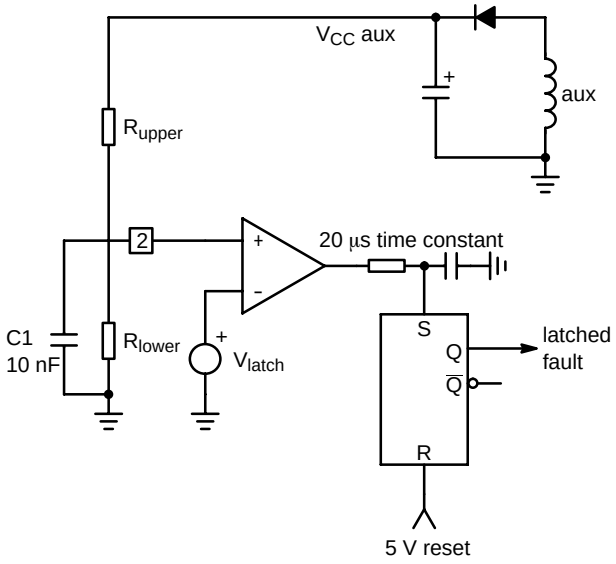


Figure 27. A Comparator Monitors Pin 2 and Latches Off the Part in Case the Threshold is Reached

Latch−off and Overvoltage Protection

Speedking features a fast comparator that permanently monitors Pin 2 level. Figure 27 details how it is internally arranged:

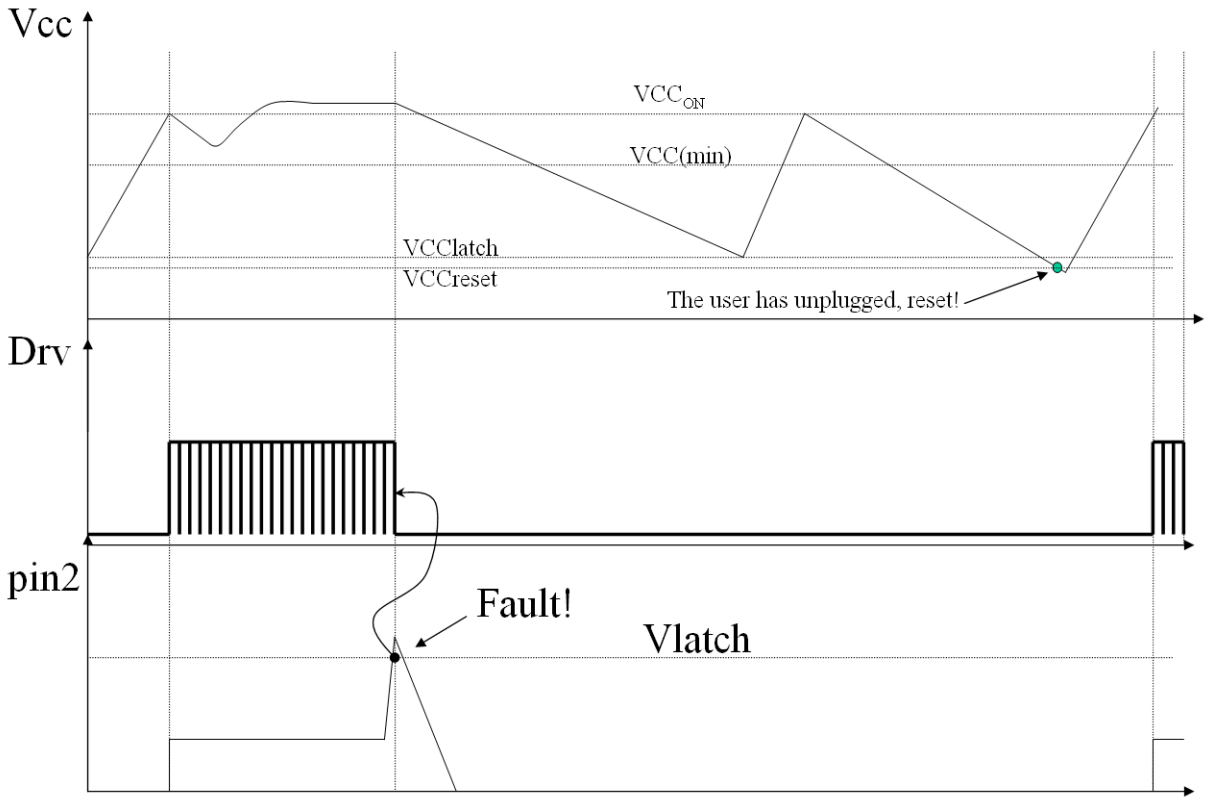


Figure 28. The Part is Reset when V_{CC} Reaches 5.0 V

If for any reason Pin 2 level grows above 3.0 V, the part immediately stops pulsing and stays latched in this position until the user cycles down the power supply. The reset actually occurs if V_{CC} drops below 5.0 V. Figure 28 details the operating diagrams in case of a fault. Please note the presence of RC time constant on the comparator output, aimed to filtering any spurious oscillations linked to an eventual noise presence. The typical value of this time constant is 20 μs.

Internal Reference Voltage

A 5.0 V reference voltage is pinned out on Pin 11 and can source up to 5.0 mA. Figure 29 details how the reference voltage can be externally used, for instance to build a precise Over Temperature Protection (OTP) circuitry. This 5.0 V source is shut down during the startup phase and goes low as soon as V_{CC} crosses $V_{CC(min)}$. It stays low during the double hiccup mode to keep the consumption to the lowest. We recommend to wire a 100 nF from this pin to ground in order to improve the noise immunity.

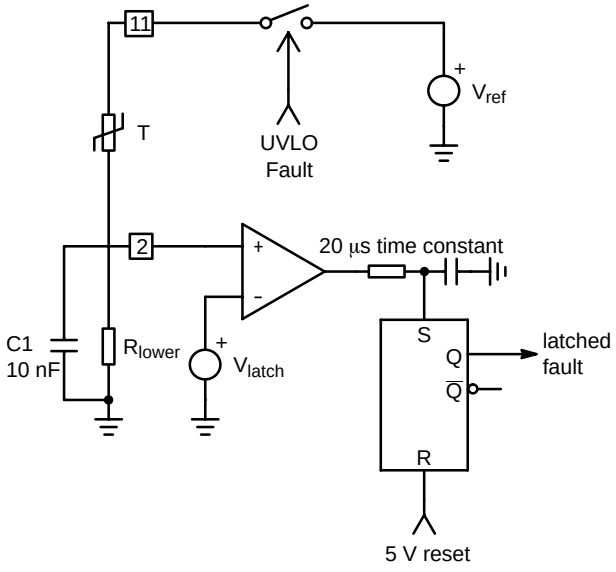


Figure 29. The Reference Voltage is used with the Latchoff Input to Trigger the Circuit in Presence of an OTP

Soft−start and Fault Timer

The Speedking features an internal soft−start circuit activated during the power on sequence (PON) but also during skip cycle to reduce the acoustical noise (see skip cycle section). As soon as V_{CC} reaches V_{CCON}, the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 1.0 V / R_{sense}). The peak current is clamped at 1.0 V / R_{sense} through the entire soft−start period until the supply enters regulation. Figure 30 shows a typical startup shot.

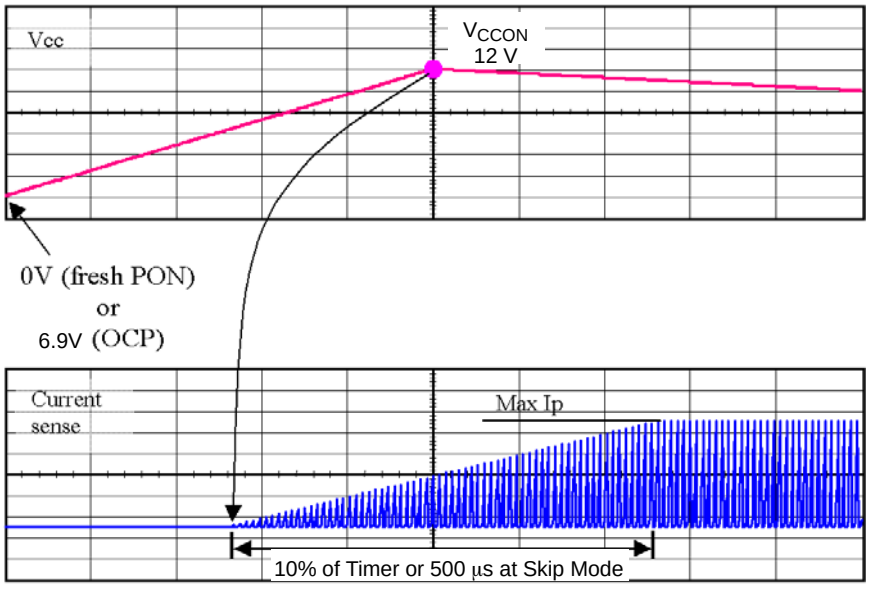


Figure 30. Soft−start is Activated During a Startup Sequence an OCP Condition (or During Skip−Cycle − 500 μs Skip Ramp)

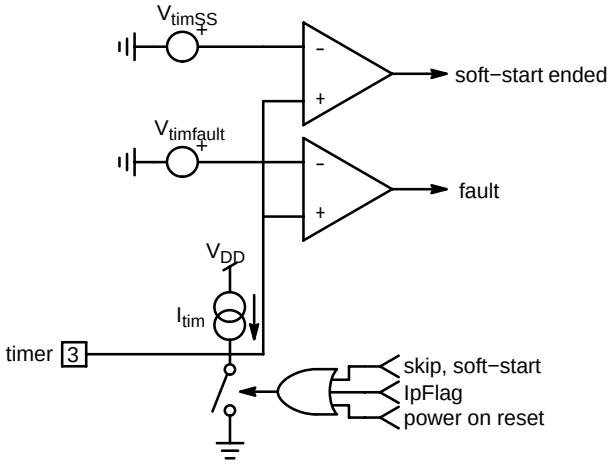


Figure 31. Soft−start is Activated During a Startup Sequence, an OCP Condition (or During Skip−Cycle − 500 μs Skip Ramp)

To simplify the circuit architecture, the timer pin also shares the soft−start comparator, as Figure 31 details. That means that the soft−start is linked to the timer duration by a ratio of 0.1 or 10% roughly. If we select a 100 ms timer period, then the soft−start duration will be 10 ms. Figure 32 details Pin 3 voltages during a soft−start sequence or a skip−cycle activity. The soft−start capacitor is reset by either the soft−start completion within the burst or by the skip comparator (500 μs Soft Skip Ramp) if the burst length is shorter than the soft−start duration.

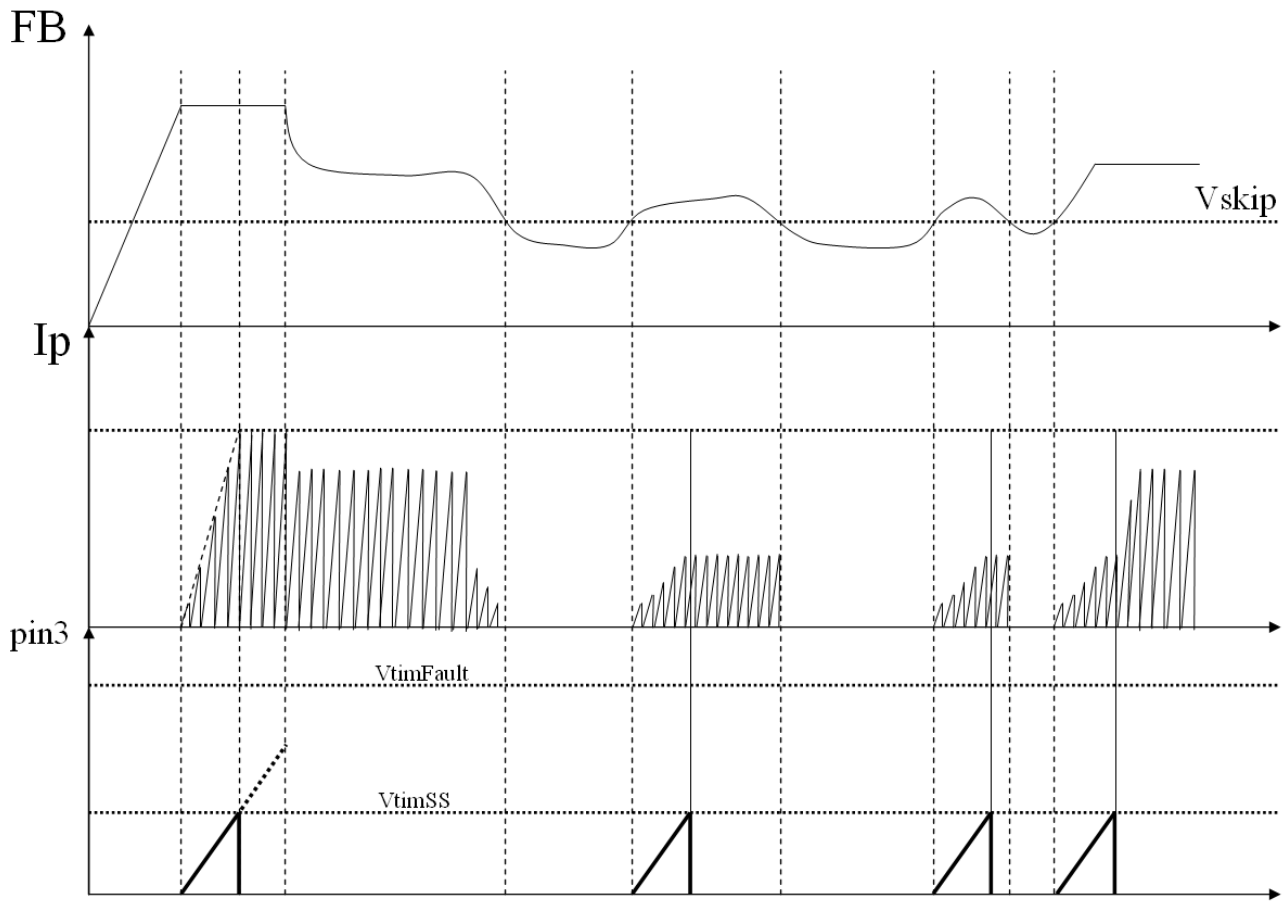


Figure 32. Soft−start is Also Activated During Skip Cycle to Offer a Smooth Current Ramping Wave Shape

How to calculate the timer capacitor value? By simply apply V x C = I x t relationship. If we look at Figure 31, we can see that the timer is completed when V_{pin3} reaches 4.0 V. If we have a 20 μA charging current and we want 90 ms of timer duration, then C is obtained by: C = I x t / V = 20 μ x 100m / 4 = 500 nF. If we select a 0.47 μF, we end−up with a final duration of 94 ms. The soft−start being 10% of this value, we will see a soft−start sequence of 9.4 ms.

Internal Ramp compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor downslope. Figure 33 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the OFF time.

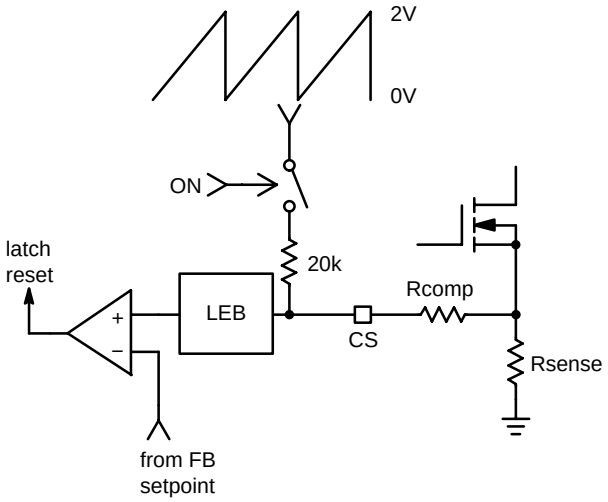


Figure 33. Inserting a resistor in series with the current sense information brings ramp compensation and stabilizes the converter in CCM operation

In the Speedking, the oscillator ramp features a 2.0 V swing. If our clock operates at a 65 kHz pace, then the oscillator slope corresponds to a 130 mV/µs ramp. In our FLYBACK design, let's assume that our primary inductance L_p is 350 µH, and the SMPS delivers 12 V with a N_p:N_s ratio of 1:0.1. The OFF time primary current slope is thus given by:

$$\frac{(V_{out} + V_f) \cdot \frac{N_s}{N_p}}{L_p} = 371\ mA/\mu s \text{ or } 37\ mV/\mu s \qquad \text{(eq. 2)}$$

When projected over an R_{sense} of 0.1 Ω, for instance. If we select 75% of the downslope as the required amount of ramp compensation, then we shall inject 27 mV/µs. Our internal compensation being of 130 mV, the divider ratio (divratio) between R_{comp} and the 20 kΩ is 0.207. A few lines of algebra to determine R_{comp}:

$$\frac{20\ k \cdot divratio}{(1 - divratio)} = 5.2\ k\Omega \qquad \text{(eq. 3)}$$

Frequency Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. Speedking offers a ±5% (±6% for DAP011C) deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with an adjustable period. Figure 34 displays the internal arrangement around Pin 4. It is actually a I – 2I generator, producing a clean 50% duty−cycle sawtooth. If we take a 1.4 V swing on the jitter capacitor, then we calculate the needed value for a 3 ms period, or a 330 Hz modulation speed, again applying the V x C = I x t relationship. We need 1.5 ms to ramp−up and 1.5 ms to ramp down, therefore: C = 20u x 1.5m / 1.4 = 21 nF. If we select a 22 nF, then our modulation frequency will be around 325 Hz. Figure 35 shows the relationship between the jitter ramp and the frequency deviation.

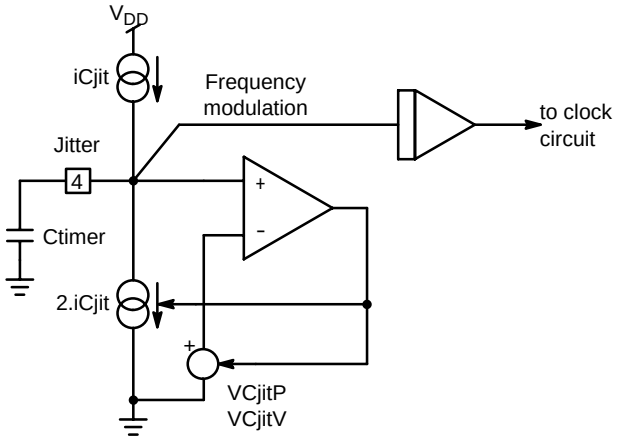


Figure 34. An Internal Ramp is used to introduce Frequency Jittering on the Oscillator Sawtooth

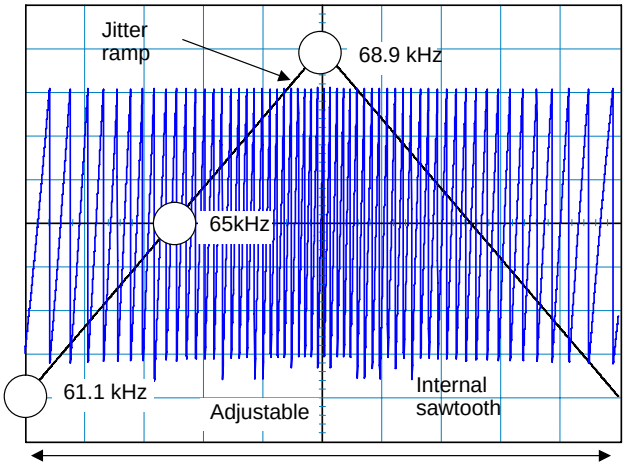


Figure 35. Modulation Effects on the Clock Signal by the Jittering Sawtooth

Skipping Cycle Mode

Speedking automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, Pin 5 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a fixed determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses. The IC enters the so−called skip cycle mode, also named controlled burst operation. The default skip cycle current is internally frozen to 30% of the maximum peak current which is 350 mV/R_{sense} The power transfer now depends upon the width of the pulse bunches (Figure 38). Suppose we have the following component values:

Primary Inductance (L_p) = 350 µH
Switching Frequency (F_{sw}) = 65 kHz
I_p skip = 600 mA (or 350 mV / R_{sense})

The theoretical power transfer is therefore:

$$\frac{1}{2} \cdot L_p \cdot I_p^2 F_{SW} = 4\ W \qquad \text{(eq. 4)}$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 4**.**
0.1 = 400 mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

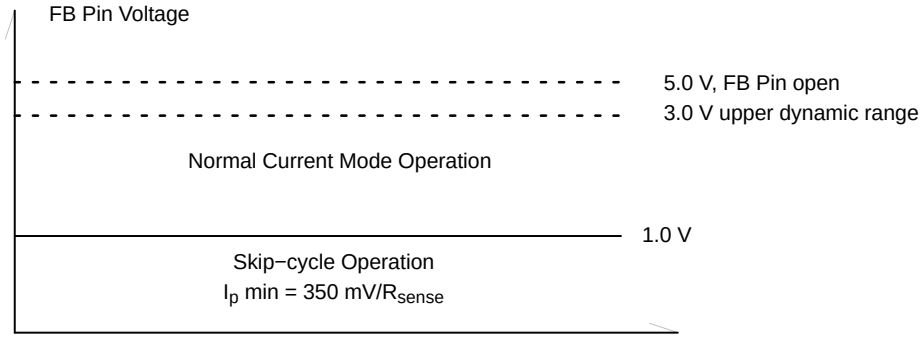


Figure 36.

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V / R_{sense}. When the IC enters the skip cycle mode, the peak current cannot go below 1.0 V / 3 or around 350 mV / R_{sense}. Figure 38 shows different values of pulse widths when the SMPS starts−to−skip cycles at different power levels:

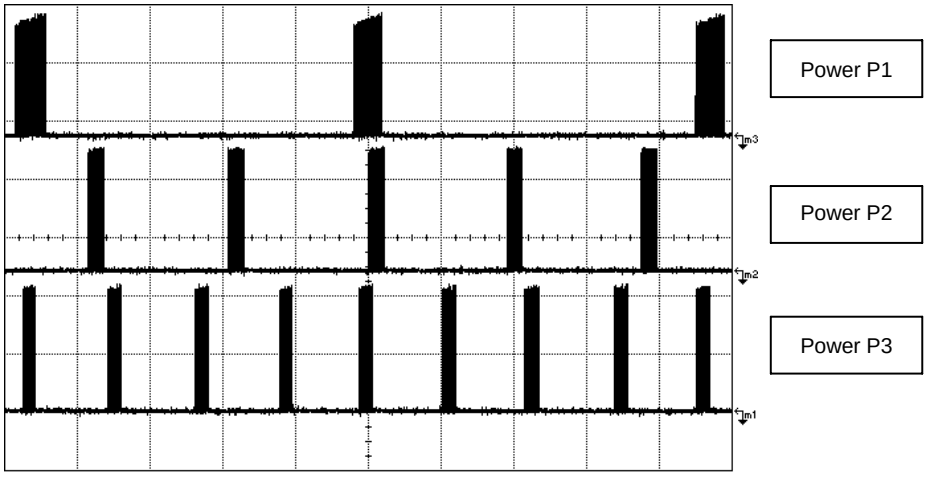
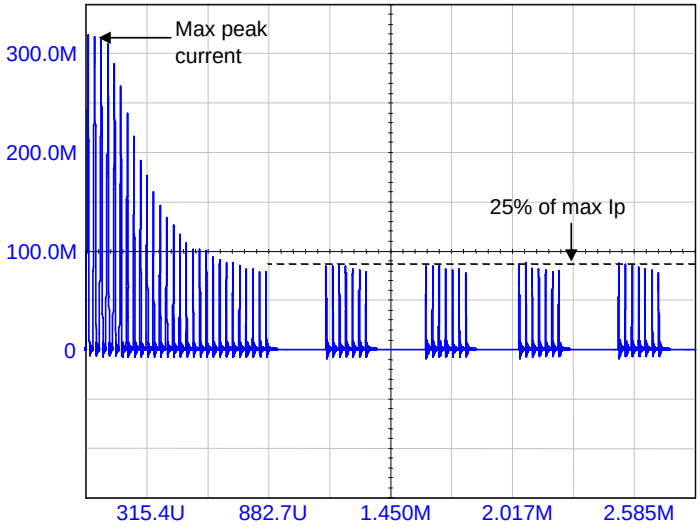


Figure 37. Output Pulses at Various Power Levels (X = 5 μs/div) P1 < P2 < P3



The skip−cycle takes place at low peak currents which guaranties noise free operation

Figure 38.

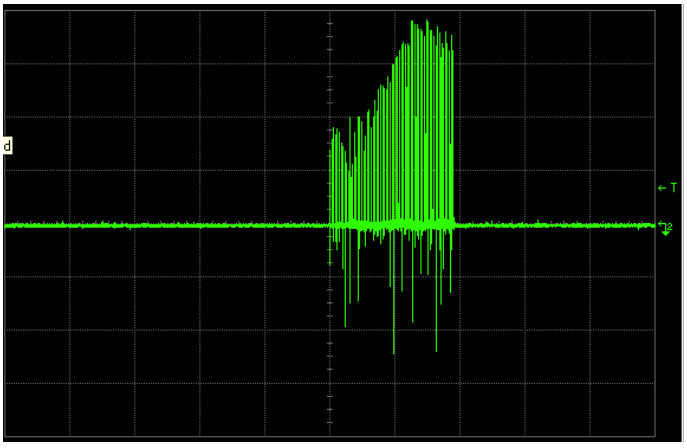


Figure 39. A Smooth Ramping Current in Skip−Cycle

As we have stated several times, the peak current in skip−cycle will not immediately ramp−up to its default value. To limit the discontinuities in the transformer mechanical structure, and thus reduce the acoustic noise, the 500 μs soft−skip ramp will be activated in skip cycle. Figure 39 shows a typical shot, showing the peak current ramp−up.

Since Pin 5 features an internal voltage source whose output impedance is 25 kΩ, it is possible to alter the default skip value. A simple arrangement consists in connecting a resistor to ground in order to lower the setpoint. On the other hand, the setpoint can be increased, if necessary, by wiring a resistor to the reference voltage. Figure 40 portrays these options.

Since Pin 5 internal impedance is 25 kΩ, it is simple to calculate the value of the resistor to decrease the V_{skip} level (1.0 V typically). Suppose we want to decrease it down to 800 mV. Then, the resistor to connect to Pin 5 is 0.8 / 40 μ = 20 kΩ. To obtain a 20 kΩ from an original 25 kΩ value, we need to parallel a (20 k x 25 k) / (25 k−20 k) = 100 kΩ.

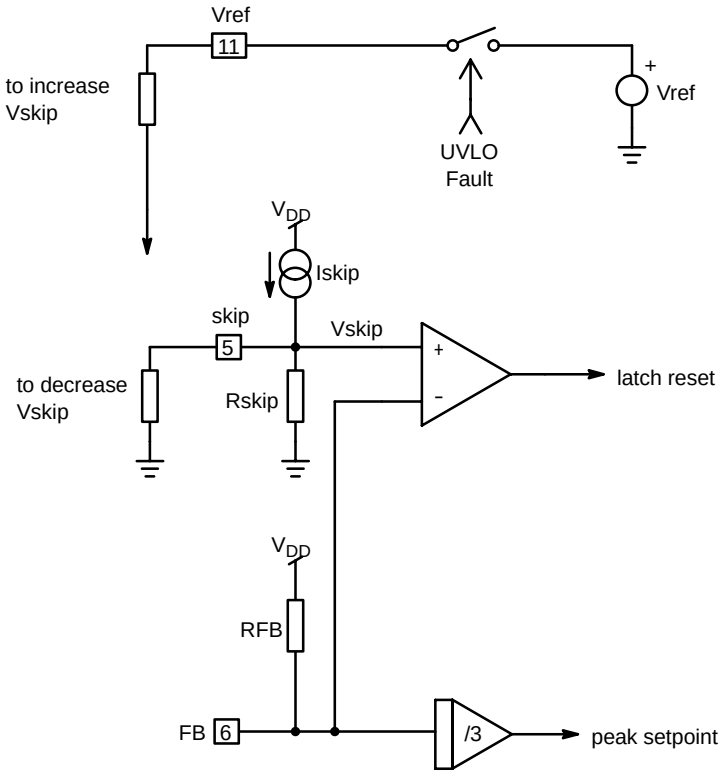
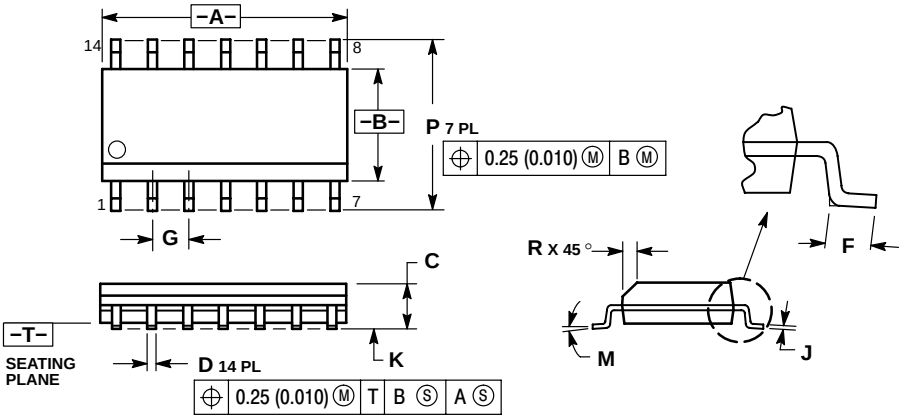


Figure 40. Due to Pin 4, it is Easy to Alter the Default Skip Level

DAP011/DAP011C

PACKAGE DIMENSIONS

SOIC−14
D SUFFIX
CASE 751A−03
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
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R	0.25	0.50	0.010	0.019

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